AND8069/D

Tips and Tricks to Build Efficient Circuits with NCP1200

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APPLICATION NOTE

Prepared by: Christophe Basso
ON Semiconductor
14, rue Paul Mesplé – BP1112 – 31035 TOULOUSE Cedex 1, France
33 (0)5 34 61 11 54
e–mail: christophe.basso@onsemi.com

Introduction

The NCP1200 easily lends itself to designing Switch–Mode Power Supplies (SMPS) in a snap–shot and its success speaks for itself. However, customers applications (and problems) are unique and often necessitate the addition of specific component arrangements around the IC. As usual, solving one particular design constraint brings another one with it, perhaps puzzling the designer even more. This application note answers typical questions that a designer can raise when starting his own system analysis, but also tries to answer some problems common to Switch–Mode Power Supply applications.

Adding an External Latching Circuit for Over Voltage Protection or Over Temperature Shutdown

When pulling NCP1200's feedback pin below the skip cycle level (pin1 voltage), output oscillations cease. If this action is accomplished through a thyristor, permanent latch–off occurs until the user cycles the Vcc down and up again by unplugging the power supply. By firing the thyristor via a zener diode connected to an auxiliary winding, an efficient Over Voltage Protection (OVP) circuit can be implemented. Figure 1 depicts the solution.

At rest, when the SMPS is properly working, Q1 and Q2 are transparent to the operations because the 10 kΩ resistors block them. As soon as the auxiliary winding level exceeds the zener voltage and fires Q2, the whole SCR turns on and via the 1N4148, pulls FB low. As a result, it immediately stops the 1200 driving pulses: the SMPS shuts off. However, the Dynamic Self–Supply (DSS) being still alive (Vcc ramps up and down between 10–12 V), the 47 kΩ resistor keeps the SCR latched despite the disappearance of the default. Once the user cycles Vcc down and up again (e.g. by unplugging the power supply from the mains outlet), the SCR de–biases and allows the 1200 to restart. Q1/Q2 could be ON Semiconductor dual combo bipolar MMBT3946DW. If for transformer noise reasons Vpin1 is much lower than its default value (1.4 V), a BAT54 must be wired in place of the 1N4148 to ensure that FB passes well below Vpin1: $Q2\_Vce_{sat}$ + Vf < Vpin1. Increasing the value of the 47 k will change the total latch–off behavior into auto–recovery mode, as the default over current protection does.

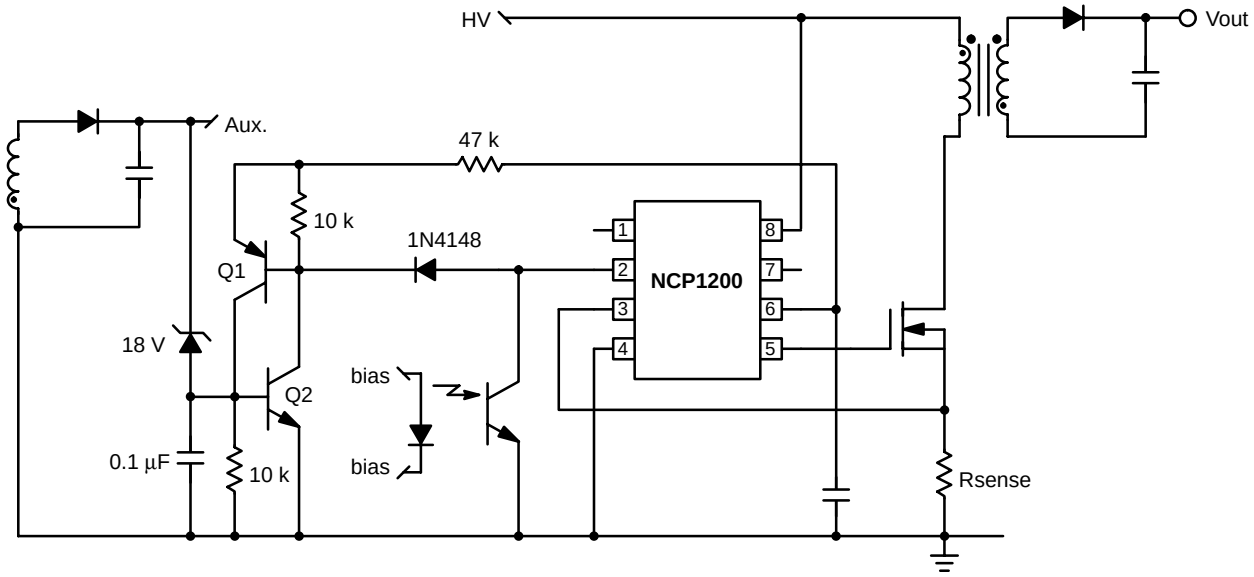

Figure 1. A Dual–Transistor Arrangement Latches–Off the NCP1200 in Case of an OVP Event

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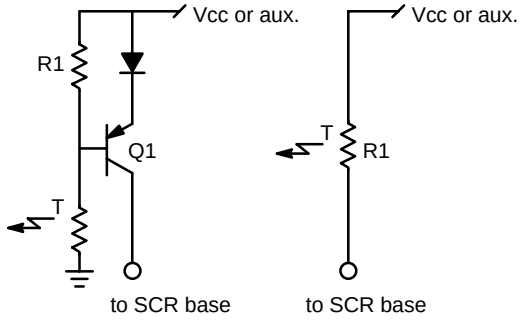

Figure 2. A NTC and a Simple PNP Make an Easy–to–Build Thermal Sensor Which Fires the SCR

A temperature shutdown can be realized on top of the above SCR by adding a PNP, as portrayed by Figure 2. The Negative Temperature Coefficient sensor (NTC) is selected to pull the PNP's base toward ground at the wanted shutdown level. To obtain slightly more dynamic on the base level, a simple diode is inserted in series with the emitter. A more economic solution involves a single thermistor, also shown on the same picture.

Driving Big Gate–Charge MOSFETs

What actually limits the NCP1200 drive capability is the DSS and not its driver stage. The driver output connects a 40 Ω resistor between Vcc and gate (see 1200 data sheet) during the ON state whereas a 12 Ω is connected in the discharge path (OFF time). If the MOSFET exhibits a large total gate charge Qg, turn–on and turn–off times will be longer but it will properly work, probably generating high switching losses. Problems usually arise because those big MOSFETs heavily load the DSS and it is important to assess the total current consumption in worse conditions. This total consumption can be evaluated through the following formula: Itotal = Icc1 + $Fswitching_{max}$ x Qg_{max}. Suppose that we use a 3 A MOSFET affected by a 25 nC Qg, then the total average current that the DSS must deliver is: 750 μA + 72 k x 25 n = 2.5 mA, if you would select a P60 version. The DSS current is 4 mA @ Tj = 25°C. However, when supplied by the high–voltage rail, the junction temperature will quickly rise, lowering the DSS capability to its minimum value stated in the data–sheet. This value being 2.8 mA @ Tj = 125°C, care must be taken that Tj stays lower than this number to ensure adequate safety margin. Needless to say that the DIP8 option offering much better thermal specs compared to SO–8, it will be preferred in high Qg applications. A good news is that the internal NCP1200 consumption significantly reduces with temperature (see characterization curves in the data sheet) and consequently eases the DSS.

Now suppose that you would like to drive big MOSFETs, featuring large Qg e.g. 60 nC or even 100 nC. It becomes impossible to use the DSS. Should you try, you would observe a Vcc that immediately collapses below 10 V after turn–on: all the current the DSS delivers is eaten by the MOSFET driving. Even if this poor situation would work, you would not be able to sense a short–circuit anymore because the function is activated only if the Vcc goes up and down, e.g. between VccOFF and VccON. As a result, using an auxiliary winding becomes the only solution. However, we will see below that the aux. winding can degrade the Over Current Protection (OCP) trip point. Figure 3 offers an interesting intermediate solution where the aux. winding plays an important role but does not bother the DSS operation, keeping the precise OCP trip point intact.

In this example, Q1 buffers the drive output and the energy necessary to drive the big MOSFET is derived from the auxiliary winding. At power–on, the DSS charges both capacitors, Caux and CVcc which are isolated by D1 as soon as the auxiliary voltage has built up above the NCP1200 VccON level. The drive current passes through Q1 and the 1200 delivers a small current to bias its base. At the opposite, D3 routes the gate current inside the 1200 as usual. A resistance can be inserted between the emitter and the gate to slow–down the turn–on transition. The no–load standby performance is better than without auxiliary winding because the only current seen by the DSS is roughly Icc1 which is low. Figure 3 clearly allows the NCP1200 to build SMPS of any output power levels, Flyback or Forward.

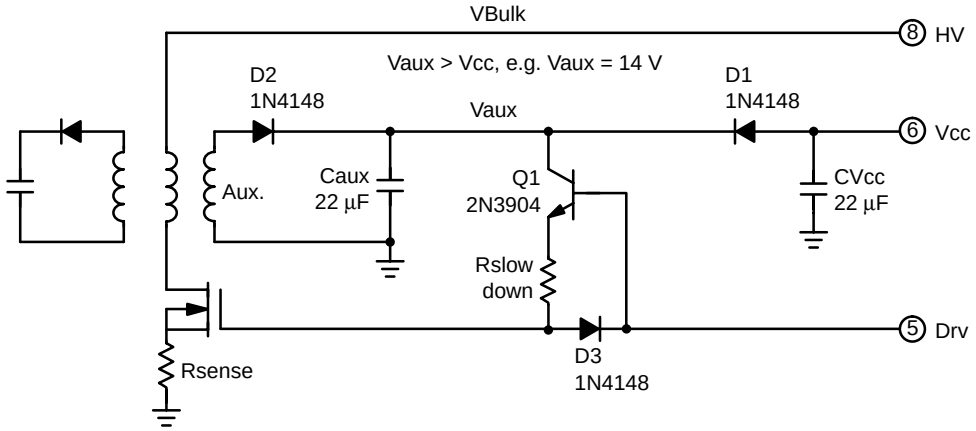

Figure 3. By Taking the Energy from the Auxiliary Winding Only at Turn–On, DSS Operation Is Not Bothered and IC Consumption Is Kept Within Safe Limits

Reducing the Standby Power with an Auxiliary Winding that Disables the DSS Operation

In certain applications, a low standby power is mandatory. This option clearly prevents from using the DSS because the 1200 supply would be the most consuming portion of the SMPS in no–load conditions. To stop the DSS, an external voltage must force the 1200 Vcc to be permanently above VccON or 11 V as given in the data sheet. Failure to reach that level would imply a DSS re–activation with all the losses in standby. Wiring the auxiliary winding with skip–cycle components can be a little tricky, especially if you target an extremely low standby power. Why? Because in standby, the pulses are not a continuous flow but a short burst whose recurrence can be as low as several tens of milli–seconds (skip cycle technique). Provided your auxiliary circuit exhibits some losses, you will not be able to maintain a self–supply above 11 V, re–activating the DSS again. Another problem takes place: the primary to secondary leakage inductance. This inductance generates a spike detected by the auxiliary diode which artificially raises the auxiliary voltage (Figure 4 with arbitrary levels). This effect can accidentally destroy the 1200 but also deteriorate the OCP detection point.

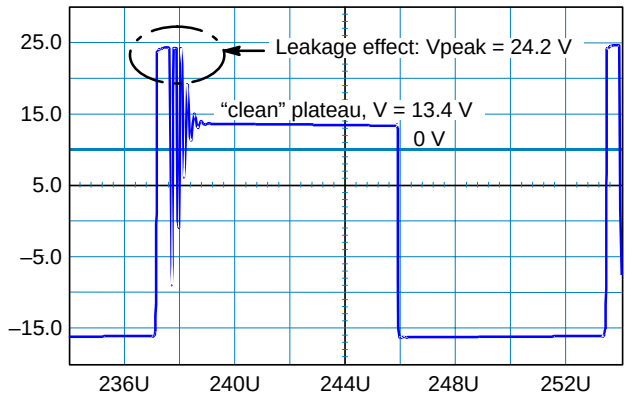

Figure 4. The Leakage Effect Seen on the Auxiliary Side Pulls–Up the Final Level Peak–Rectified by the Diode

As the NCP1200 Vcc cannot exceed 16 V, care must be taken at the design stage to limit the voltage excursion while running nominal load. A good solution would be to first integrate the leakage spike and then rectify the wave with a diode as Figure 5 suggests. Unfortunately, in standby, the auxiliary level would collapse because the burst energy is so low that the 22 Ω would dramatically limit the 22 µF re–fuelling current. We will exploit this feature in a later application.

The solution consists in splitting the rectifying section in two blocks, the second one clamping Vcc below 16 V. This solution is depicted by Figure 6. The BAT54 is only here to avoid hampering the startup time by charging two capacitors together. If this is not a problem, you can simply omit it. The zener voltage can be lowered but the maximum VccOFF (12.5 V) must be reached otherwise the 1200 won’t startup.

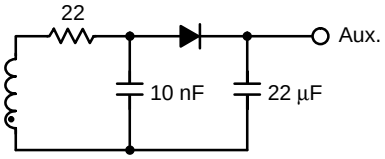

Figure 5. A Resistor and a Capacitor Can Integrate the Perfidious Leakage Inductance

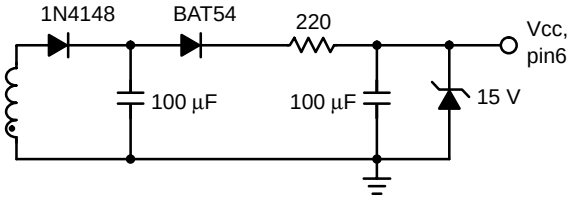

Figure 6. This Configuration Ensures Self–Supply in Standby and Prevents Vcc from Exceeding the 16 V Maximum Rating

Using an auxiliary winding as wired according to Figure 6 offers true short–circuit protection but the precise over load mode detection brought by the DSS is lost. This is imputed to the primary leakage inductance, which in some cases is so energetic, that a short on the secondary power winding cannot drop the auxiliary winding, preventing short–circuit detection. Reducing the primary clamp level (via the RCD network) represents a good solution, but to the detriment of the efficiency. If this is a problem in your application, below are other solutions keeping all the 1200 goodies with an auxiliary winding.

A 70 W demo board was built using an auxiliary supply and revealed less than 100 mW standby power at 350 VDC input level.

Using Auxiliary Winding Without Affecting the OCP Trip Point, but Disabling the DSS

One great aspect of the DSS, is the fact that the OCP circuitry is activated whatever the auxiliary voltage is, because it does not use any! In low standby power applications, you will need to wire an auxiliary winding to permanently disconnect the DSS. Unfortunately, the 1200 internal OCP circuitry activates when Vcc crosses VccON (≈ 10 V) while going down. This action naturally takes place with the DSS, but if you wire an auxiliary winding, it just disappears because you managed to keep Vaux above 10 V to invalidate the DSS. As a result, if you overload the output, NCP1200 will activate its burst only when the auxiliary Vcc collapses below 10 V. And what happens if you have a poor coupling between the windings and a large primary leakage inductance (see Figure 4)? You never detect the OCP.

We have seen that the leakage inductance generates an energetic spike that couples to the auxiliary winding. Why not sampling the auxiliary voltage on the plateau, a short time further to the leakage appearance? This is exactly what Figure 7 circuit does for you.

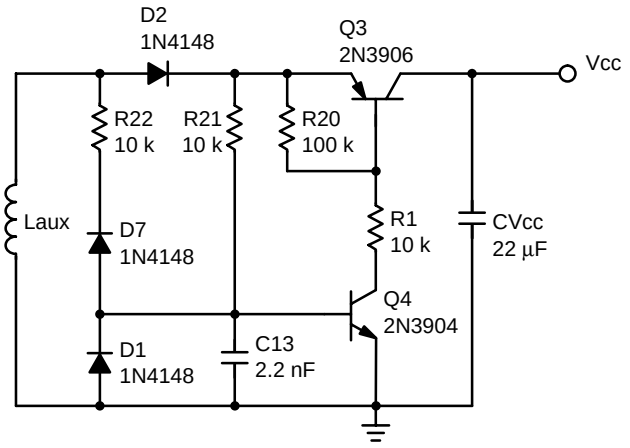

Figure 7. The Delay Introduced by Q4 Samples Right After the Leakage and You Obtain a Nice DC Voltage

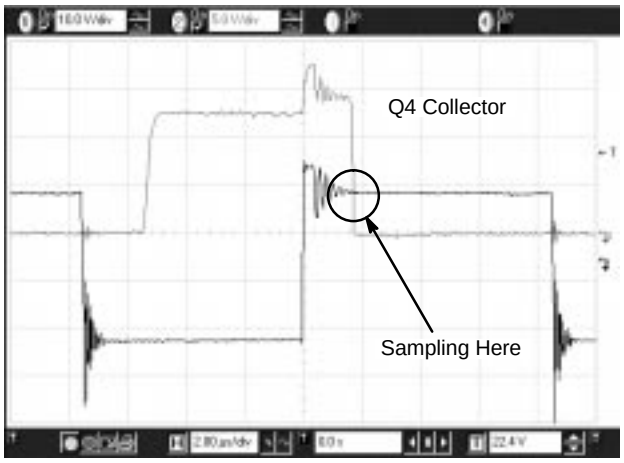

Figure 8. By Delaying the Sampling Time,You Obtain a Clean Auxiliary Level Without Any Leakage Effect

When the main power switch is ON, capacitor C13 is discharged through R22 and D7 whereas D1 avoids a deep reverse bias of Q4 base–emitter junction. When the main switch opens, the secondary voltage sharply rises and node 1 becomes positive. However, C13 being discharged, Q3 stays open and Vcc does not grow up. After a short period of time (adjustable through R21 or C13), Q4 closes and brings Q3's base closer to ground. Vcc now goes up and catches up node 2 level, minus Q3's Vce sat. If the time delay is correctly selected, Vcc is absolutely clean from any voltage spike because you have sampled the plateau.

Figure 8 details the scope shot obtained using this circuit. As you can see, the sampling time occurs right after the leakage and the auxiliary level extracted from this plateau is clean. This solution can also be very useful in application where precise primary regulation is needed.

With this solution, the off–time is truncated to avoid the leakage effect. In standby, when skip cycle takes over, this off–time is considerably reduced and our delay circuit loses quite a bit of precious energy: the auxiliary winding collapses and cannot self–supply anymore the 1200. To combine the advantages of a clean self–supply (remember, to get a precise overcurrent trip point or a good primary regulation level if any) together with excellent standby power performance, Figure 9 offers an interesting solution. The schematic becomes more complicated but has been tested fine.

Q1 and Q2 perform their duty as described above but when voltage is present over C2, Q3 is biased and keeps D8's anode low enough to block it. When the supply enters standby, C2's level goes low and unleashes Q3 which can now let the current flow through D8, keeping 1200 self–supplied in standby. As soon as the load comes back, Q3 closes again and C2 recovers its role.

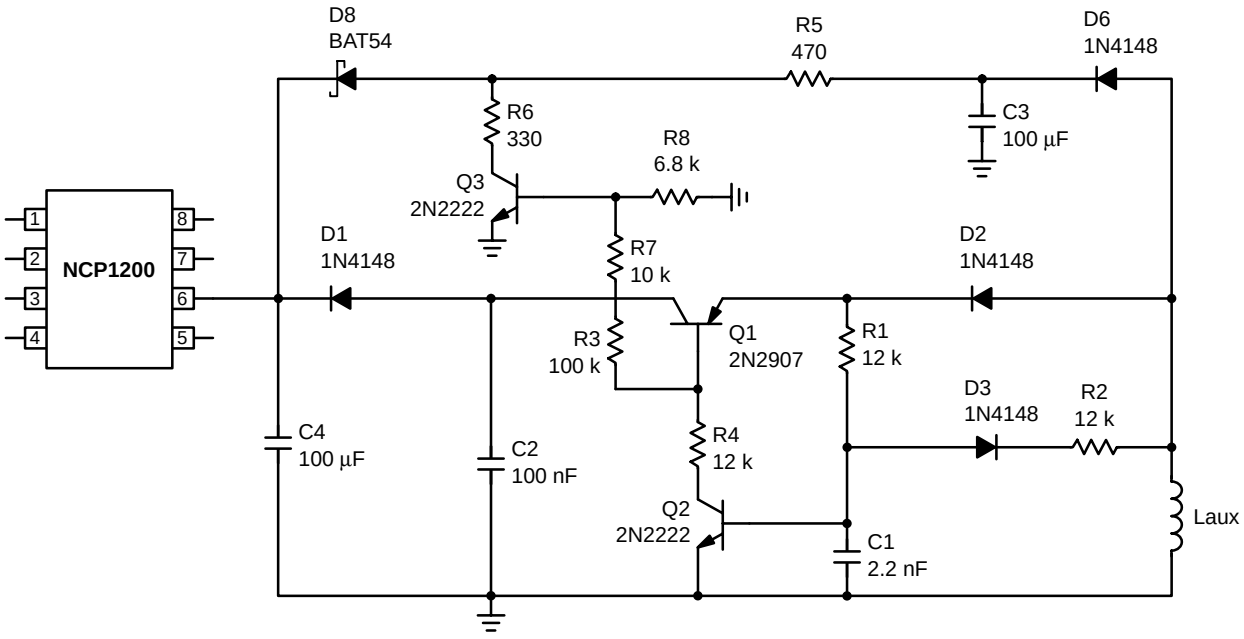

Figure 9. A Shunt Prevents the Auxiliary Level to Supply the 1200 in Normal Operation But Becomes Active in Standby

Using Auxiliary Winding Without Affecting the OCP Trip Point and Keeping the DSS Working

The DSS offers a very interesting feature which is the ability to implement true overload detection. Standard UC384X–based systems are usually built with an auxiliary winding but because of the poor cross–regulation between the windings, it is almost impossible to implement a precise over load protection. However, these systems can usually cope with short–circuit constraints because the auxiliary winding finally collapses when Vout equals zero. (See Figure 4 to see who is guilty.) As such, the DSS is a very desirable choice when true over load protection is required by the customer. Unfortunately, in no–load conditions, the DSS being connected to the high–voltage rail, you directly measure this power consumption on the input, despite the low current consumption of the 1200. In some very stringent standby power requirements, you simply cannot accept these losses. Figure 10 presents a solution built on top of that presented in Figure 3.

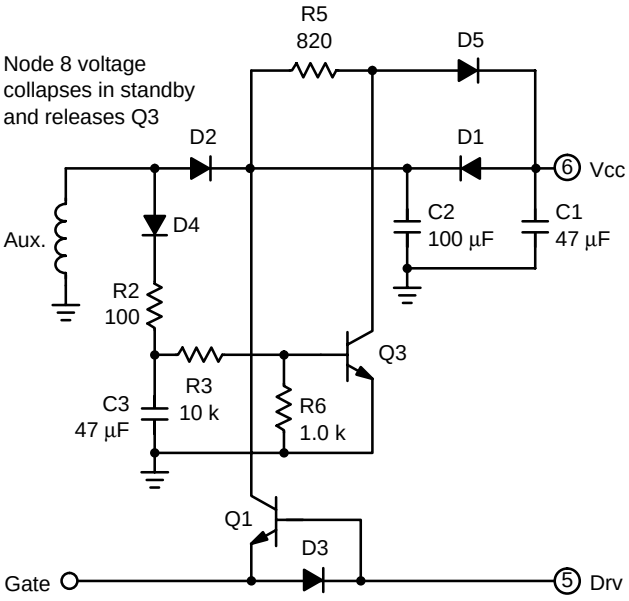

Figure 10. This Solution Upgrades Figure 3 Option by Disabling the DSS in Standby

The trick used to detect the standby or no–load condition, is to take benefit from the the weak energetic content of the burst pulses when the supply operates in standby. That is to say, if the refueling current circulating through D4 is diminished by a resistor (R2), then C3 will never be able to maintain a normal operating voltage (e.g. as the one at nominal load) and it we be severely reduced. In the example, we measured 15 V in normal load, and less than 3 V in standby. In normal operation, C3's voltage is high enough to forward bias Q3 via R3/R6. His collector pulling R5 terminal to ground, D5 is naturally blocked and the DSS plays its role: precise over load mode detection, and EMI jittering through its ripple. When the SMPS goes to standby, C3's level decreases until Q3 gets un–biased. Its collector no longer pulls R5 to the ground and D5 can pass all the auxiliary level developed across C2 to block the DSS. R5 value can be adjusted to avoid too much of wasted power as long as D5 stays blocked in nominal load operations. The standby power becomes as good as stated before: less than 100mW at high line. Thanks to this latest solution, you can:

- Drive the MOSFET of your choice: all the ON current is drawn from the auxiliary winding.
- Benefit from the DSS activity to build a precise over current detection and use its ripple for EMI jittering.
- Disable the DSS in no–load conditions and obtain one of the best standby power on the market.

Inserting a Resistor with Pin8 to Avoid Over–Dissipation of the Package

Some users like to use the SO–8 package mainly because of its small size. Unfortunately, the thermal resistance junction–to–ambient makes the exercise difficult because the DSS naturally dissipates heat (except if use some alternative solution as depicted below). The auxiliary winding option is still possible, but the best Over Current Protection (OCP) trip point is obtained with the DSS. The DSS being active, there is no other alternative than dissipating this heat through copper, or, move it to another component, e.g. a series resistor. By inserting a resistive element in series with pin8, every time the DSS turns on, you drop some voltage across the resistor (Figure 11) . You thus spread the total power between two components instead of one, lowering NCP1200 Tj inside the SO–8 package. The calculation is easy. You know by the data sheet that every time the DSS turns on, 4 mA flow inside pin8 at steady–state. If one keeps about 50 V minimum on pin8 to properly operate the DSS, the resistor value can be calculated through:

$$Rdrop \leq \frac{Vbulk\,min - 50}{4\ m}$$

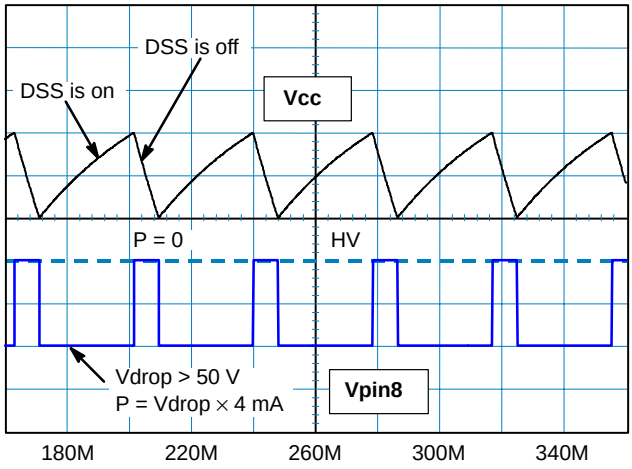

Figure 11. By Inserting a Resistor with Pin8, You Can Split the Power Between an Active and a Passive Component in Order to Keep Tj Lower

Below are two examples showing the benefits of inserting the resistor.

Case 1:

Single mains, 230 VAC ± 15%, NCP1200 average consumption is around 2.5 mA. DSS duty–cycle is 62%. Vbulk max = 374 VDC and Vbulk min = 276 VDC. Rseries = (276 – 50)/4 m = 56 kΩ.

1. Without the resistor, NCP1200 would dissipate (worse case): 374 x 2.5 m = 935 mW, incompatible with the SO–8. With an RtetaJA of 100°C/W, the maximum power the NCP1200D version can handle at an ambient of 40°C is: 125°C – 40°C/100 = 850 mW
2. By inserting the 56 kΩ resistor, we drop 56 k x 4 m = 224 V during the DSS activation. The power dissipated by the NCP1200 is therefore: Pinstant x DSS duty–cycle = (374 – 224) x 4 m x 0.62 = 372 mW. We can pass the limit and the resistor will dissipate 935 – 372 = 563 mW.

Case 2:

Universal mains, 90 – 27 5VAC, NCP1200 average consumption is around 2.5 mA. DSS duty–cycle is 62%. Vbulk max = 388 VDC and Vbulk min = 127 VDC. Rseries = (127 – 50)/4m = 19 kΩ.

1. Without the resistor, NCP1200 would dissipate (worse case): 388 x 2.5 m = 970 mW, incompatible with the SO–8.
2. By inserting the 19 kΩ resistor, we drop 19 k x 4 m = 76 V during the DSS activation. The power dissipated by the NCP1200 is therefore: Pinstant x DSS duty–cycle = (388 – 76) x 4 m x 0.62 = 773 mW. We can pass the limit and the resistor will dissipate 970 – 773 = 197 mW.

“When I Insert a Resistor in the Gate of My MOSFET, the Supply Becomes Instable”

The Leading Edge Blanking (LEB) circuitry has the role to clean the voltage appearing across the sense resistor. By discharging all the parasitic capacitors at turn–on, you create a current spike that can engender false tripping of the current comparator. To avoid this problem, NCP1200 includes a LEB calibrated at 250 ns. The LEB starts to blank the current sense information as soon as the driver goes high. Figure 12 displays the drive and gate signals when a resistor inserted between gate and driver is small. This represents a normal operating conditions where the gate follows the driver. However, inserting a larger resistor in series with the gate is a common practice when one wants to slow down the main switch, e.g. for EMI reasons. Unfortunately, the resistor delays the turn–on of the MOSFET and truncates the Leading Edge Blanking (LEB) which no longer plays its role (Figure 13). In that case, false triggers occur and instabilities takes place. The cure consists in adding an RC network between Rsense and the current sense pin (Figure 14).

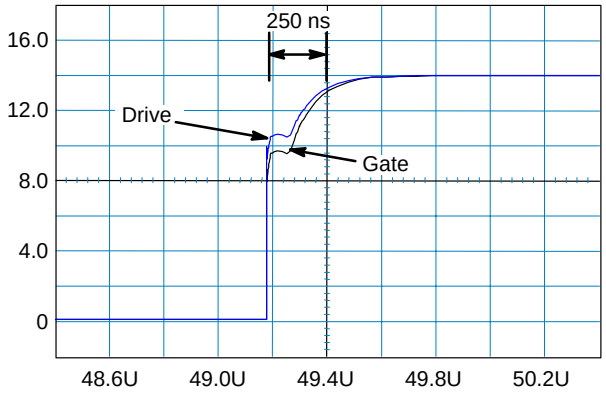

Figure 12. When the Gate Follows the Drive, the LEB Works Fine

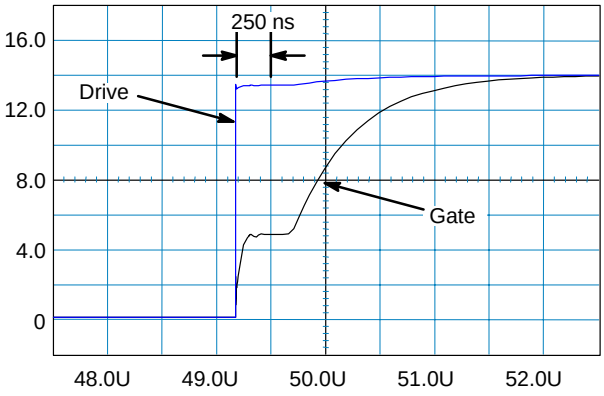

Figure 13. Delaying the Gate–Source Signal Produces the Effect of Truncating the LEB

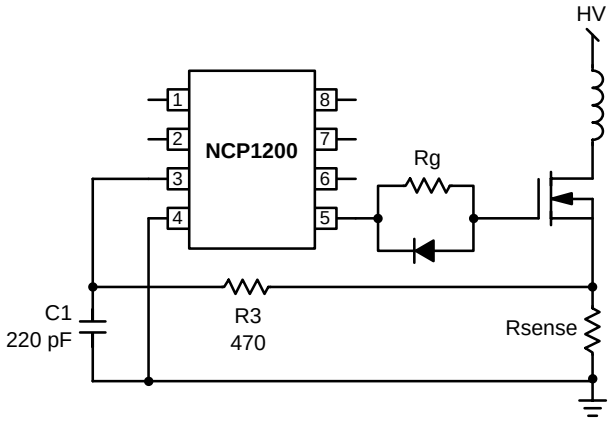

Figure 14. This Network Re–Enforces the LEB Action by Integrating the Sense Signal Whatever the Gate Delay

“What MOSFET’s Size Can I Drive in Half–Wave Configuration?”

In some of the available application notes, we propose to wire pin8 not to the bulk capacitor but to the rectifying half–wave. This solution is acceptable for low gate–charge MOSFETs only, because the DSS current capability is

divided by two in average (half–wave duty–cycle is around 50%). As a result, the DSS can only deliver 2 mA DC which divides between the controller (Icc1) and the driver consumption, utilized to charge up the MOSFET's Qg. If we take the very worse case that appears at high temperature, the DSS minimum current is 2.8 mA which divided by two makes 1.4 mA. Removing Icc1 (≈750 μA, this number goes down when Tj goes up), we have 650 μA with 100 μA left to charge the Vcc capacitor. As a result, with a 60 kHz version, the maximum Qg would be: 550 μA/60 k = 9 nC. This corresponds to a 1 A MOSFET or a 2 A MOSFET featuring low gate charge only. If you wire a bigger MOSFET, Vcc will collapse without the classical ripple 2 V due to the DSS operation. No ripple means no OCP because the 10 V error flag test has gone. (See application note AND8023/D for more detailed explanation.) In summary, we recommend half–wave operation only in configurations that guarantee proper DSS operation at any temperature.

"I Have Routed My 1200 with a Large Copper Area Around the Package. What Power Can I Dissipate?"

The maximum power accepted by the NCP1200 is given by:

$$Pmax = \frac{Tj\,max - Tamb\,max}{R\theta J - A}$$

As you can see, you could define yourself two parameters in the formula: Tj*max* given by the data sheet, or the maximum operating temperature your Quality Department fixes, and finally Tamb*max*, given by your application. Unfortunately, you cannot determine RθJ–A because the copper area you added has actually changed it from the original data sheet specification. The best is to measure it with a simple method that has proven to be accurate enough for our purposes. First, you need a bare PCB featuring the copper area you have routed. It can be your final board without anything soldered on it. Then, you solder the NCP1200 (DIP8 or SO, depending on your selection) directly on the copper (please, without a socket). Once this is done, we need to find a Temperature Sensitive Parameter (TSP) to evaluate the junction temperature inside the package. One of the internal ESD zener diode represents a good choice. Before using it, we must calibrate it. Several solutions exist but the easiest one is to take a multi–meter in diode position offering sufficient resolution (3 or 4 digits are ok) and current stability during the measurement. The Agilent HP34401A can be a possible selection. The ESD diode connected to pin1 can be used but another one could also be wired, e.g. the current sense pin. Now, bias it in forward mode by connecting probe + to the ground and probe – to pin 1. At an ambient of 25°C, you should read something like Vf ≈ 720 mV. The rest of the operation requires a precisely controlled heater to calibrate our junction. Put the NCP1200 under the heater's bell and measure the Vf at different points, e.g. every 10°C. At every step, wait at least a few minutes that the reading stabilizes before recording the point. If everything goes well, you should obtain a linear graph as Figure 15 shows.

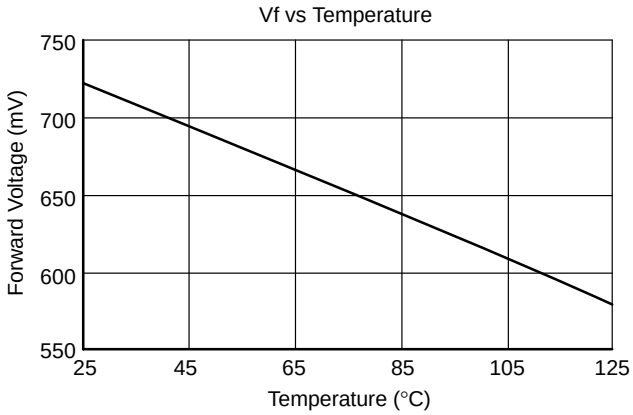

Figure 15. Collecting Data Points and Feeding a Spreadsheet Unveils the ESD Junction Temperature Behavior

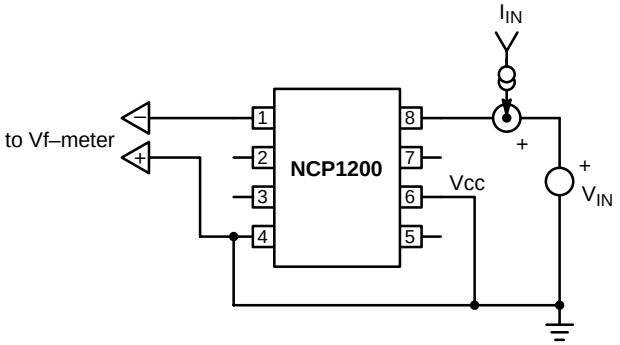

Figure 16. Next Step Is to Inject Power Into the Chip

With that graph on hand, we can now start measuring our RθJ–A. On the same PCB board, make a short between Vcc and ground, leave all the other pin open but keep the Vf–meter connected. Do not bring too much of solder on the joints to be in same final industrial conditions (for instance wave soldering). Now, bring a DC source to pin8, normal polarity, that is to say, pin8 positive by respect to ground. Figure 16 shows the wiring diagram for best understanding where an ampere–meter has been inserted. Immerse all the 1200 PCB test fixture into an hermetic oven and select the ambient temperature at let's say 40°C. Turn the DC power supply on and start to increase the voltage. At a certain moment, the DSS turns on and the ampere–meter indicates a current. Increase the voltage until you reach a power value of 300 mW roughly (V_in x I_in). Leave everything cooking for a while, until the Vf reading stabilizes. You will note that the current goes down a bit because of the DSS thermal effect (actually self–protective). After time has elapsed, suppose that you read Vf = 652 mV and Ptotal = 280 mW. From Figure 15, we extract the corresponding junction temperature given by our calibrated TSP: 652 mV → Tj ≈ 75°C. From these numbers, we are able to calculate our thermal resistance junction–to–ambient resistor by:

$$R\theta J - A = \frac{Tj - Tamb}{Ptotal}$$

which turns to be 125°C/W. A few remarks concerning the measure:

- Use a well temperature–controlled oven. Failure to stabilize the temperature in a quiet environment will engender large errors.
- Wait that the part has stopped its temperature excursion before taking the Vf point. DIP8 packages require longer time than SO–8.

"What Power Level Can I Expect from the NCP1200?"

The NCP1200 being a general purpose current–mode controller, you can virtually use it in any applications ranging from a few hundred of mW up to 100 W or more! The above design ideas will let you implement the solution best adapted to your application. The limiting factor is actually the power switch and the 1200 driving capability. In the simplest application schematic (no aux. winding) with the DSS working and a 3 A MOSFET featuring low gate charge, we have successfully built a 70 W universal mains application board exhibiting 81% efficiency at low line and 87% at high line. Associating an auxiliary winding and a single or dual bipolar stage (as described in the data sheet) will let you drive the MOSFET of your choice, e.g. a 10 A device, reducing the conduction losses and the heatsink size.

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