Intusoft Newsletter

Personal Computer Circuit & System Design Tools

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New: 64-bit IsSpice4

Intusoft is pleased to announce its release of the new 64-bit version of its IsSpice4 circuit simulator. With proven benchmarks on average of 32% decrease in simulation run time, Intusoft has launched its most advanced SPICE technology yet. Smaller designs to large, analog to mixed-signal, the time-savings and efficiency with 64-bit IsSpice4 is remarkable and cost saving for users.

64-bit operating systems for Windows have been in existence since 2001, but they became popular in 2005 when Microsoft released their Windows XP Professional x64 Edition. This adjoined with Visual Studio 2005, which supported 64-bit processors.

Intusoft managed to port the IsSpice4 simulator to the 64-bit system in 2006. However, we were not satisfied with the outcome of the port, as limitations on operating systems of the time did not allow for much improvement in simulation performance. The only advantage was the ability to simulate larger circuits, due to the 64-bit addressing scheme. That version was not officially released since we did not see any realistic advantage over the 32-bit version. Since then, some other manufacturers released 64-bit versions of their analog circuit simulators, but the claims about speed and accuracy improvement were quite exaggerated and rarely realized by designers.

The new release of Intusoft's ICAP/4 design simulation programs come with two batch files that instantly switch your executables between the 32-bit or 64-bit versions. Of course, the 64-bit version can only be run on 64-bit CPUs, under a 64-bit operating system. The 32-bit version is compatible with any Windows operating system. The simulation version, as shown below, is at the bottom of the of the simulation screen.

If you are running on a 64-bit operating system, we recommend using the 64-bit version of IsSpice4, with adequate RAM (4GB or more) to get the full benefit of the software. Running 64-bit IsSpice4 on a native 64-bit architecture will allow it to perform all memory operations natively, and avoid the transition penalty that a 32-bit version has on a non-native operating system.

Starting with Visual Studio 2010 code, this could be compiled with flags specifically set to take advantage of the AVX (Advanced Vector Extension) capabilities of the new CPUs. Of course, one has to be careful not to pay the transition penalty when mixing legacy code with SSE and the new instruction sets. This all has enabled us to incorporate the best accuracy and speed for users. In fact, we have observed more than a 40% decrease in total simulation time going from the 32-bit to a 64-bit version on some power supply designs.

Let's now run some simulations to compare the two versions of IsSpice4.

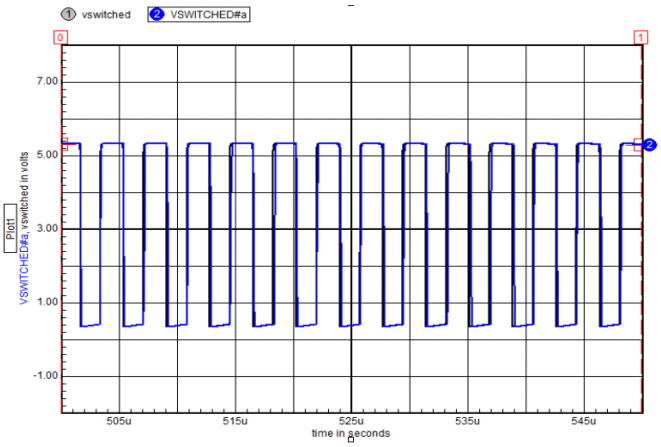
First, try running the NCP1570.dwg in the "\spice8\Circuits \power\ON Semi Demo Templates" folder, using both the 32-bit and 64-bit versions, then compare results. This is a fairly simple low voltage buck controller, and is powered from 12V. It uses two MOSFETS to produce an output of 1.18V over a wide range of currents. The final simulation results from the 32 and 64-bit versions of IsSpice4 are virtually identical, but the 64-bit version gives you a 19% improvement in simulation speed.

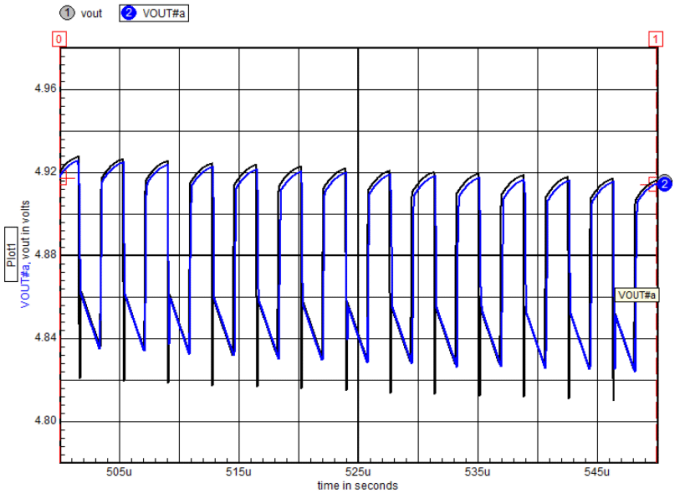
Next, let's move to a more advanced design by running the CS5307.dwg from the previous folder. This circuit is an advanced buck converter. The controller has four gate drivers driving the four phases. It produces a 1.5V output form a 12V input, while providing 80A on 18.75 Ohms. The working frequency is between 200 and 800KHz. The results from the two different versions are pretty much identical, but the 64-bit version again improves the speed of the simulation by 18%.

To show the full advantage of the 64-bit version of IsSpice4, let's now run the CS5171.dwg located it the following folder:

"\spice8\Circuits\powerDemo\ON Semi Demo Templates"

This is a boost converter, which features the On Semi CS5171 switching regulator with a high efficiency 1.5A integrated switch. The flexibility in the design of this part allows it to operate in most power supply configurations, including boost, flyback, forward and buck. Run this circuit with both 32 and 64-bit versions and confirm that the 64-bit version finishes 44% faster than the 32-bit version, and without any loss in accuracy as shown in the figures below.





The table below provides a comparison of total simulation time, and the resulting improvement, by running the 64-bit version on some of the most common power supply designs. These are located in the following folder from your installation.

\spice8\Circuits\power\ON Semi Demo Templates

Circuit Name	32-bit run time(sec)	64-bit run time(sec)	Improvement %
CS5171.dwg	44.8	24.6	44
CS5308.dwg	69.43	53.17	23
MC33262.dwg	20.55	15.25	26
MC34063A BUCK 12V to 3.3V.dwg	12.47	9.47	24
NCP105X Buck.dwg	13.28	9.15	31
NCP105X Flyback.dwg	51.7	39.92	23
NCP1203 100kHz Flyback.dwg	18.5	13.03	30
NCP1205P with OVP.dwg	11.32	7.62	32
NCP1570.dwg	24.23	19.63	19
sum	266.28	181.84	32

On the large IC design side we ran a few simulation on MCNC large circuit netlists and came up with the following table.

All times with a Core i7-3520M @ 2.9GHz , 8G RAM and running Win10

Circuit Name	32-bit run time(sec)	64-bit run time(sec)	Improvement %
ADD32.ckt	97.05	73.83	24
PCHIP.ckt	18.72	13.5	27
SRAM.ckt	46.72	34.23	25
VOTER25.ckt	59.23	45.83	22

The above .ckt files are included in your new installation folder under
\spice8\Circuits\MCNC\netlists

Analyzing the Scott T Transformer Connection

Beginning with Coulomb in the late 18th century, the theory of electricity began to unfold. The 19th century became the golden age of discovery with Ampere, Oersted, Gauss, Weber, Faraday, Maxwell and many others describing the behavior of electricity and magnetism. Toward the end of the 19th century, the American entrepreneurs began to exploit the science with Edison and Westinghouse, battling to assert leadership in the move to electrify the world. Tesla, then working for Westinghouse after a fallout with Edison over using AC power, won the patent battle with Ferraris over the rights to the invention of the AC motor. Edison was losing his battle for DC, even though he mounted a blistering political attack on the "unsafe" AC technology. As the AC distribution took hold, there was still competition over the best frequency and whether 2-phase or 3-phase was best.

About the same time, one of the earliest "circuit design" patents awarded to Charles F Scott in 1894 described a transformer connection that became known as the Scott T. It converts 3-phase to 2-phase power and vice versa. Still in use today, this circuit is the featured topic of this newsletter. Its configuration changed over the years since the original patent was awarded[1]; but it remains substantially the same. The schematic of Figure 1 shows the connection used to power a Y connected 3-phase load from a 2-phase source.

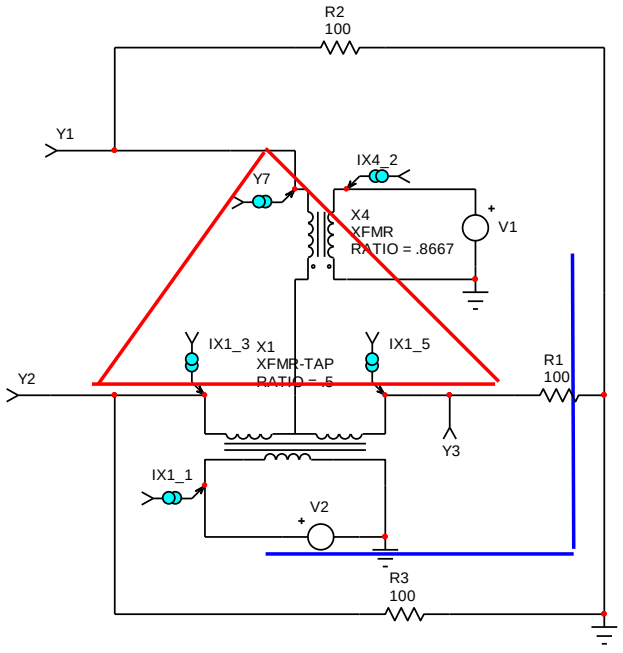


Figure 1, Scott T and vector diagram

The Blue axis represents the 2 phase vectors, the vertical being the imaginary sine axis and the horizontal the real or cosine phased axis. The red triangle represents the delta-connected phasor. Here's an opportunity to learn about a few capabilities of our SpiceNet schematic system. First, notice the test points attached to the transformer subcircuit nodes. These use the 6y hotkey to attach a current test point to a subcircuit. SPICE primitive parts all allow you to view current passing through them. The 6y test point adds that capability to subcircuit models. You can view the current and voltage waveforms to confirm the circuit works as advertised. Next, we will construct two new schematics to see what happens when square waves are used for the input and another version to see how capacitive loaded rectifier circuit's current spikes are reflected into the 2-phase source. First use SpiceNet's layered configurable schematic to make the new configuration, all using the same schematic. Here are the layers and configurations that make up the new schematic.

Table 1, Layers are combined to make schematic configurations

	sine	square	rectifier
main	✓	✓	✓
sine	✓		✓
square		✓	
resload	✓	✓	
rectload			✓

Begin by making the layers (main, sine,…) shown in the above table using the options>>layers menu. Then send the load resistors to the 'resload' layer and the sine generator to the sine layer. To move items to another layer, select them and right-click >> "Move Item to Layer". Then make the configurations (sine, square, rectifier) from the layers as shown in the table. Select the square configuration and add the square wave generators. SPICE does not have a square wave generator with zero average value. We have a library element that does the job using two PULSE voltage generators. Just press x to browse the library and use the one found in

!generators>>!Pulse>>VGEN.

That makes a sine-phased component. To make a cosine-phased component, place another generator in the horizontally phases position and double click to open its properties dialog. Click on the SUBCKT item and it will show a button called 'enter'. Click the button to view the subcircuit; it's partially shown below in Figure 2. After the {period} parameter in V1 and V2, enter 90; that's the phase delay for a voltage source, delaying it by 90 degrees to make it cosine aligned.

```
* Period Signal period in Seconds
V1 hi v12 PULSE {Initial} {Pulse+Initial} {0} {Rise} {Fall}
+ {Duty/100*(Period-Rise-Fall)} {Period} 90
V2 v12 lo PULSE {Initial} {Initial-Pulse} {Period/2} {Rise} {Fall}
+ {Duty/100*(Period-Rise-Fall)} {Period} 90
```

Figure 2, Partial VGEN Subcircuit Netlist

Press OK to save the revised subcircuit. Your modification will only be applied to the instance that you selected. To setup the transient analysis, press the button to the left of the setup field in the toolbar. Select "Transient" and enter 1u for the data step time and 10ms for the transient analysis time. Press ok, then select "Simulator Options", and select itl4. Change its value to 0. That tells the simulator to automatically adjust itl4, resulting in faster run time. Then check the VSECTOL option, changing its value to 1u. That controls the time step such that the change in node voltage multiplied by the time step is less than 1 V-msec. Both of these options were introduced by Intusoft to improve the speed and accuracy of the SPICE simulation. You are now ready to perform the simulation by pressing the running man icon in the toolbar. Looking at the .out file; you will see that Maximum Transient Iterations were 3.

The 3 line-to-neutral waveforms are shown in Figure 3. As you can see, the phase-shifted waveforms, Y2 and Y3, are quasi-square waves, and each has the same RMS value. The primary currents are square waves with the same RMS current, in-phase with the generating voltage. The inability of

the circuit to maintain the secondary voltage wave shape suggests the rectifier spikes will produce different current waveforms in the 2-phase primary. The schematic for the rectifier configuration is shown in Figure 4.

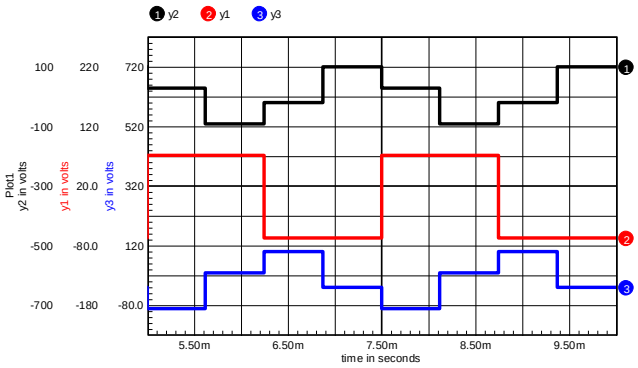


Figure 3, Quasi-square waves approximate the phase shifts

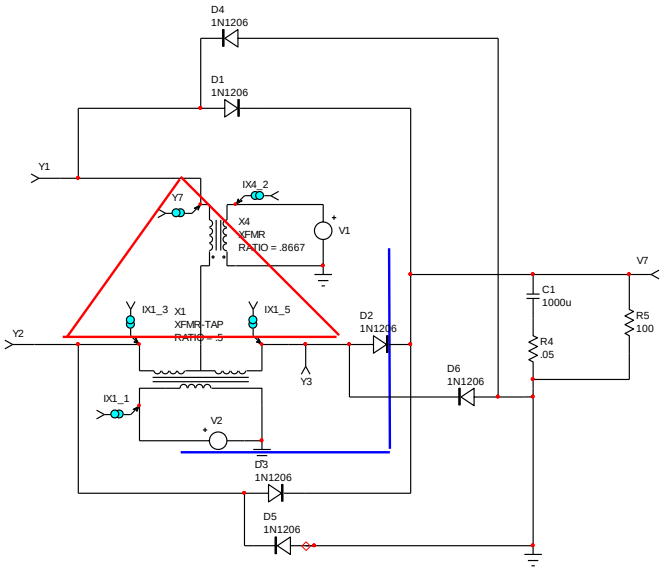


Figure 4, Scott T with capacitive rectifier load

For this simulation, more accuracy is needed to resolve the output voltage, so VSECTOL was set to 1u. To illustrate the ease of viewing waveforms with different convergence options, try setting method to gear, and reltol to .01. Run again. Then, select “Add Updated Doc” to immediately see the new waveforms.

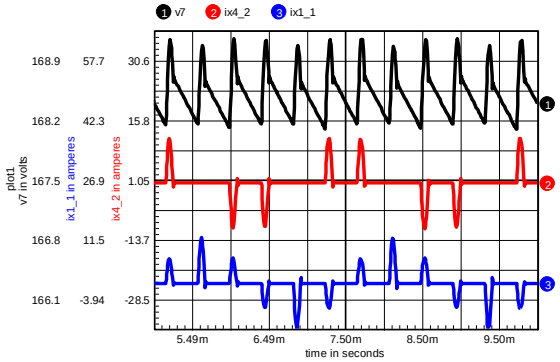
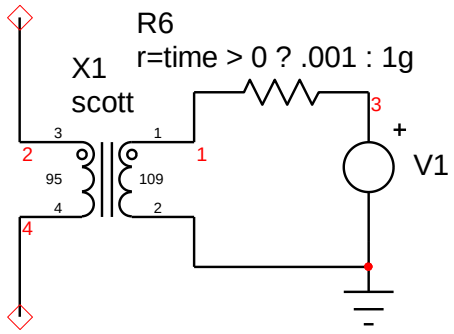


Figure 5, Output voltage and input current

The average power delivered to the “Teaser” transformer from V1 is about 8% higher than from V2.

For the next exercise, you use these simulation results to build the transformers using Magnetics Designer. Magnetics Designer needs the RMS AC winding currents to account for copper loss. Start Magnetics designer and select the core, EI Lamination 6mil Square. That should give an acceptable core loss at 400 Hz. In the Transformer tab, Enter 400 Hz for the frequency and press ‘Add’ at the lower left to bring up 2 windings. For winding 1, enter 110 for Volts Avg. Specified and 3.0 Amps for the AC Current. Then add 95.4 Volts and 3.4 Amps for the next winding. Change the insulation wrapper to 10m and press Apply.

To get a higher efficiency, select a larger core in the Core tab and check Lock Geometry. Then in the transformer tab, check ‘new’ and press Apply. When you are happy, open the IsSpice tab and press Add to Library. You can find the model in the library by searching for the name you gave it. Now replace the ideal transformer with this one and save the schematic as scott_T_real.dwg so you don’t overwrite the original. Now we are almost ready to simulate; however, you must get the initial conditions right. The cosine waveform initializes to a high voltage, and that will initialize the magnetizing current to a large number. That results in an apparent DC component, so you must make sure the Teaser transformer is initialized properly. You can do that by inserting a switch between V1 and the transformer that closes after the simulation starts. Placing a resistor in series with V1, which changes value from 1g to 1m, does the trick.



Figures 6, R6 initializes X1 properly

Run the simulation to verify your models. Then design a main transformer and place its model in the Scott_T_real.dwg. The new simulation was run for 100ms and data delayed until 95ms to settle out the start-up transient. Finally check the current in the 2-phase primary. Notice the RMS current is smaller and the waveforms have wider and smaller peaks. That's because real-world resistance and inductance were added to the model. In this case, it actually helps increase the power factor and efficiency.

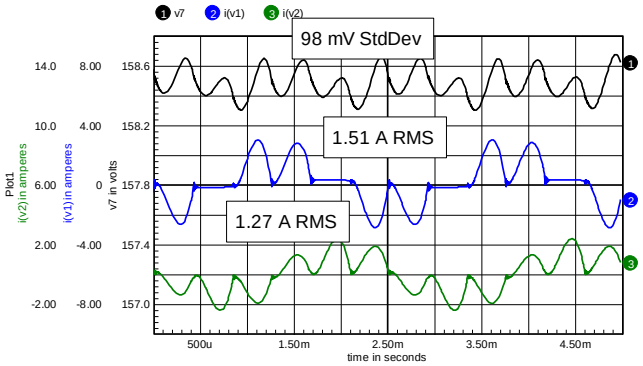


Figure 7, Adding an accurate transformer model shows lower ripple current and higher efficiency

Output power is 251 Watts, at 158.4 VDC. Overall efficiency was measured as 95.2%, and 21% more power was delivered from V1 through the teaser transformer.

[1] Patent US520975 June 5, 1894

Controlling the Internet of Things

Circuit design has become intertwined with computer science to such an extent that circuit design engineers must also master the art of computer programming, and integrate human interface design into their creations. This is evident when devices are connected wirelessly as part of the Internet of Things, IoT. We will explore some of the issues and challenges for designers of this new technology.

For the first part in a series of articles, we start with a low-power end device. IoT devices are frequently operated from the AC mains, continuously drawing standby power. In the USA, standby power consumes over 50 watts per household at a cost of over $65 per year. With scores of new IoT devices added to this standby power, it is imperative that standby power per device be reduced substantially below 1 Watt per device.

Just how much power is needed to switch an AC mains load? Using an optically coupled Triac, a short 5 mA pulse does the trick, and several mAmps more powers a micro control unit. The major power requirement becomes the radio transceiver. IEEE 802.11 WiFi uses in the neighborhood of 2 Watts. But the newer 802.15 brings bandwidth and power consumption to more reasonable levels

The best technology for now is the Microchip MRF89XAM9A-I/R that runs from 3.3 VDC, requires 3 mA standby to operate the receiver and 25 mA to transmit. The transmit operation is infrequent so some of the power can be drawn from a capacitor. The net result is we can get along quite nicely with a 15 mA, 3.3 VDC power supply. Now, we may also want to operate some 5 VDC devices; for example, the Triac control circuits. So a low dropout, LDO, regulator is used to convert 5 VDC to 3.3 VDC. Both the MCU and Transceiver have hibernate modes that brings power down to under 1 uA. So an end device can keep alive indefinitely using a small 3 VDC coin Battery when AC mains power is not available.

Low power applications like this one can sneak power off the AC mains using a capacitor-rectifier combination. The simplified schematic is shown in Figure 2.1 and the simulation results (simple.dwg) are shown in figure 2.2

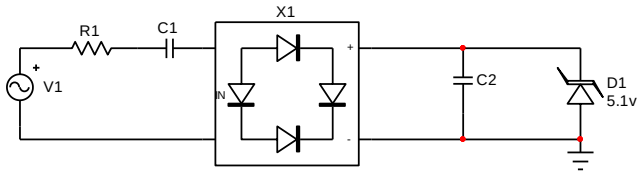


Figure 2.1, Low power capacitor-rectifier power supply

This circuit is easily configured for EU power, 50Hz at 230 VRMS, by reducing C1 and increasing R1. EU designs will also use different transceiver frequencies and outlet styles, making their designs unique rather than universal.

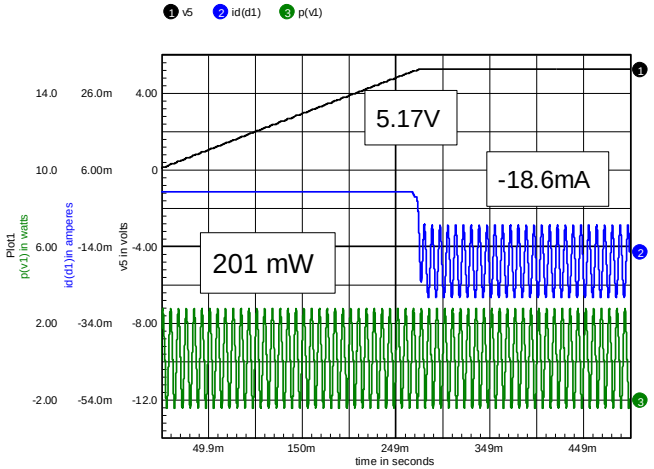


Figure 2.2, Simulation results for R1=180 Ohms, C1=.47uF and C2 = 1000uF

Notice that the circuit ground is different than the AC mains return. That will require power derived from an isolation transformer for testing. Our standard test setup adds 1kW halogen lamps in series with the High side of the AC mains to act as a short circuit current limiter. The Zener diode, D1, acts as a shunt regulator. Capacitor C1 is a low voltage, high capacity electrolytic capacitor that supplies peak transmitter current. C1 is a polypropylene capacitor that limits the current and R1 limits transient power. Average power drawn from the AC mains is 201 mW, costing about 25 cents per year, which is well below the current 1 W suggestion for small appliances. The C1 value is fairly common for EMI filters. The power factor is very low and capacitive because of the C1 ballast. But, that's not the whole story. For the rest of the story, we need a more complex simulation. First, the power needs to be switched on when the AC mains are at peak voltage, in order to measure the transient power dissipation in R1. C1 needs some series resistance to match the ESR of the electrolytic capacitor and a 3.3 VDC regulator circuit is needed. Finally, a coin battery and

switching load must be simulated. All of this is shown in Figure 2.3.

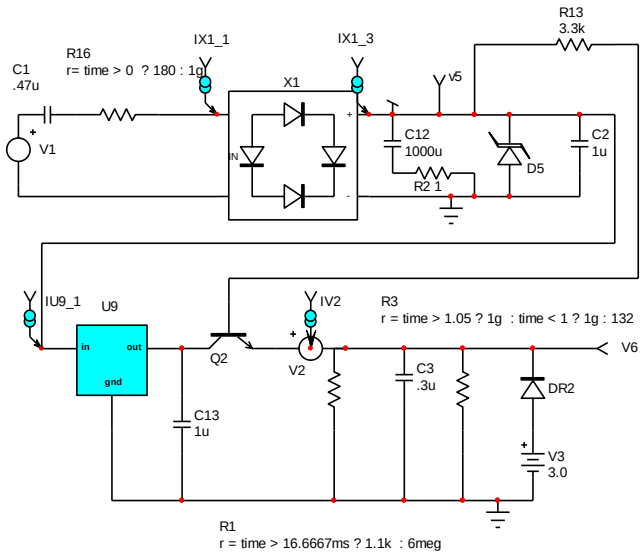


Figure 2.3, The compete power supply with simulation control switches and test points

Q2 and R13 prevent the LDO regulator, U9, from loading the coin battery, V3, when the AC mains are down. Resistors R16, R1 and R3 change values during the simulation, using the if-then-else notation commonly found in programming languages like C and PHP. We could have used a behavioral switch model, but that would have required extra pulse generators to control the switches. The if-then-else controlled resistor is unique to IsSpice4 recognizes time as a variable denoting simulation time. In this simulation, the AC mains stay OFF for one complete cycle, then switch ON along with a 3 mA load, R1. A transmit pulse is simulated between 1 and 1.05 seconds. C3 represents 3 bypass capacitors used for the micro control unit and radio transceiver. Table 1 shows the standby conditions measured at time = 15 msec. Table 2.2 gives the standby power when the AC mains are ON, measured at 99 msec.

Table 2.1, Standby power in hibernation with AC mains OFF

VDD(3.3 V)	2.9503V
I(V2)	-7.1469pA
I(V3)	-.804uA
V5	10nV

Table 2.2, Standby power with AC mains ON

VDD(3.3 V)	3.18
I(V2)	3.2mA
I(V3)	179nA
V5	5.1V
Pin AVG	200mW
I(D5) AVG	-15.3mA

Simulations were run for 2 seconds and need to be accurate to around one percent. For circuits controlled by switched nonlinearities, it is convenient to use the simulation setting shown in Table 2.3. This switches IsSpice into VSECTOL controlled time steps. VSECTOL is a unique IsSpice4 setting that is a counterpart to the SPICE CHGTOL, something akin to flux tolerance but using the Voltage time product instead. Reduction in VNTOL, ABSTOL and RELTOL relax the SPICE defaults to favor VSECTOL control. Setting ITL4 to 0 commands IsSpice4 to figure out this value automatically. Gear integration accommodates switched nonlinearities better than the default trapezoidal integration. ITL4 is the number of iterations to converge before reducing the time step. Other simulators must set this very high to get through strong nonlinearities, dramatically increasing simulation time. Ok, if you don't mind waiting hours for a simulation to complete, go ahead and use pSpice!

Table 2.3, Simulation settings

ABSTOL	1n
ITL4	0
METHOD	Gear
RELTOL	.01
VNTOL	10u
VSECTOL	30n

Resistor R16 limits peak power when a transient occurs on the AC mains. Usually a MOV is used to limit the peak voltage spike, but if R1 were very small, C1 would differentiate the spike rise time causing upset level currents to flow along the ground plane. Moreover, the transient power level must be considered in sizing R16's power handling capability. Using

http://www.vishay.com/docs/20043/crcwhpe3.pdf

we find the maximum power to an 85 usec (R16*C1) pulse is about 700 Watts which is less than the 160 Watt peak measured at turn-on; allowing for operation with a 350 V MOV to limit AC mains transients.

Figure 2.4 shows the overall simulation with annotated measurements. One of the tricks, using IntuScope to find average values of repetitive waveforms, is to place the left cursor near the time position where you want to take the average, then press the 'w' key. That will measure frequency and place the cursors 10 cycles apart. Then press the 'a' key after selecting various waveforms to measure the average value. You can also use the 'r' key to measure RMS, the '$' key for standard deviation (RMS with a average removed); that's what you would read using a true RMS AC Voltmeter.

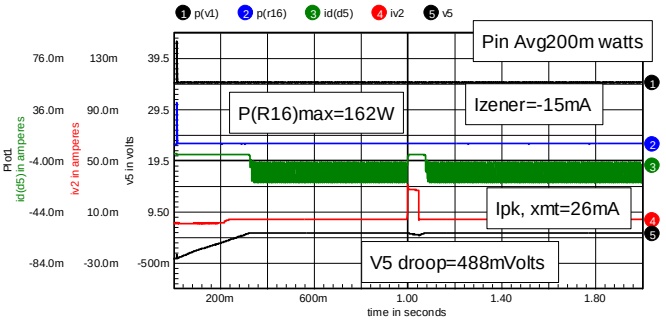


Figure 2.4, Annotated simulation results

This is the opening article in a series that takes you through a system that controls devices belonging to your IoT. We will alternate between software and hardware. The next newsletter will feature an Intranet based controller. You can look ahead at lowpan4u.com, our eCommerce site and read the Welcome page found by opening lowpan4u.com/products_tour.php and taking the tour.